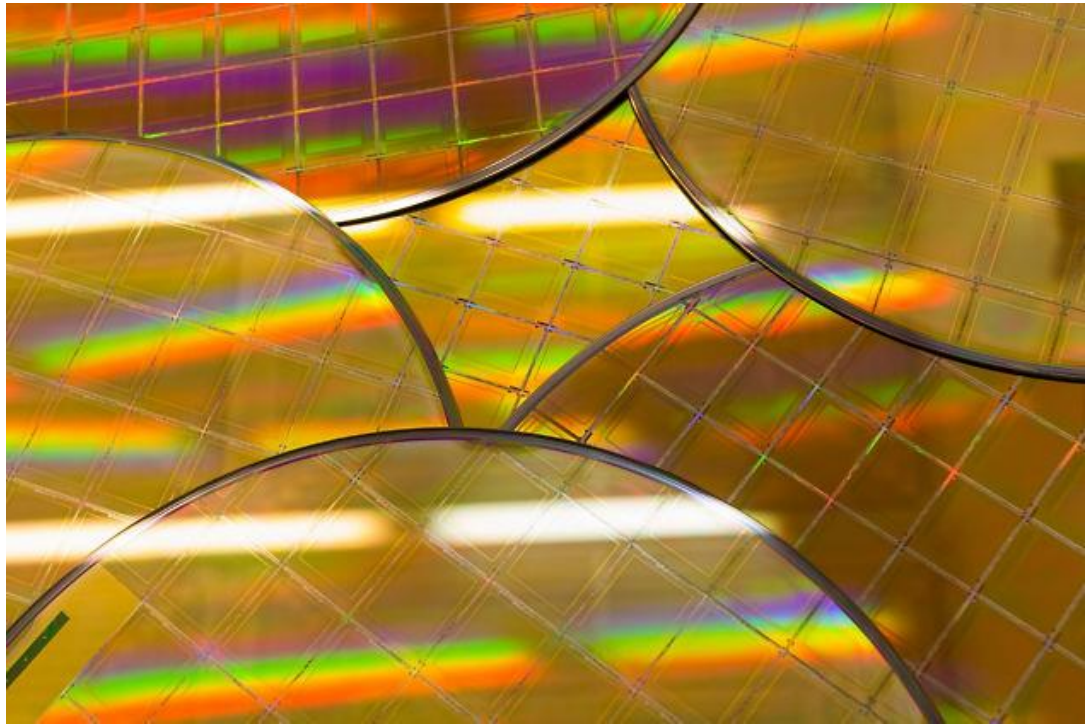
Designing Foundry-Compatible Photonic Components and Circuits



Presented by:

Greg Baethge, Team Lead – Photonics Application Engineering
Ansys Lumerical

July 13th, 2025

Tower Semiconductor
Where Analog and Value Meet

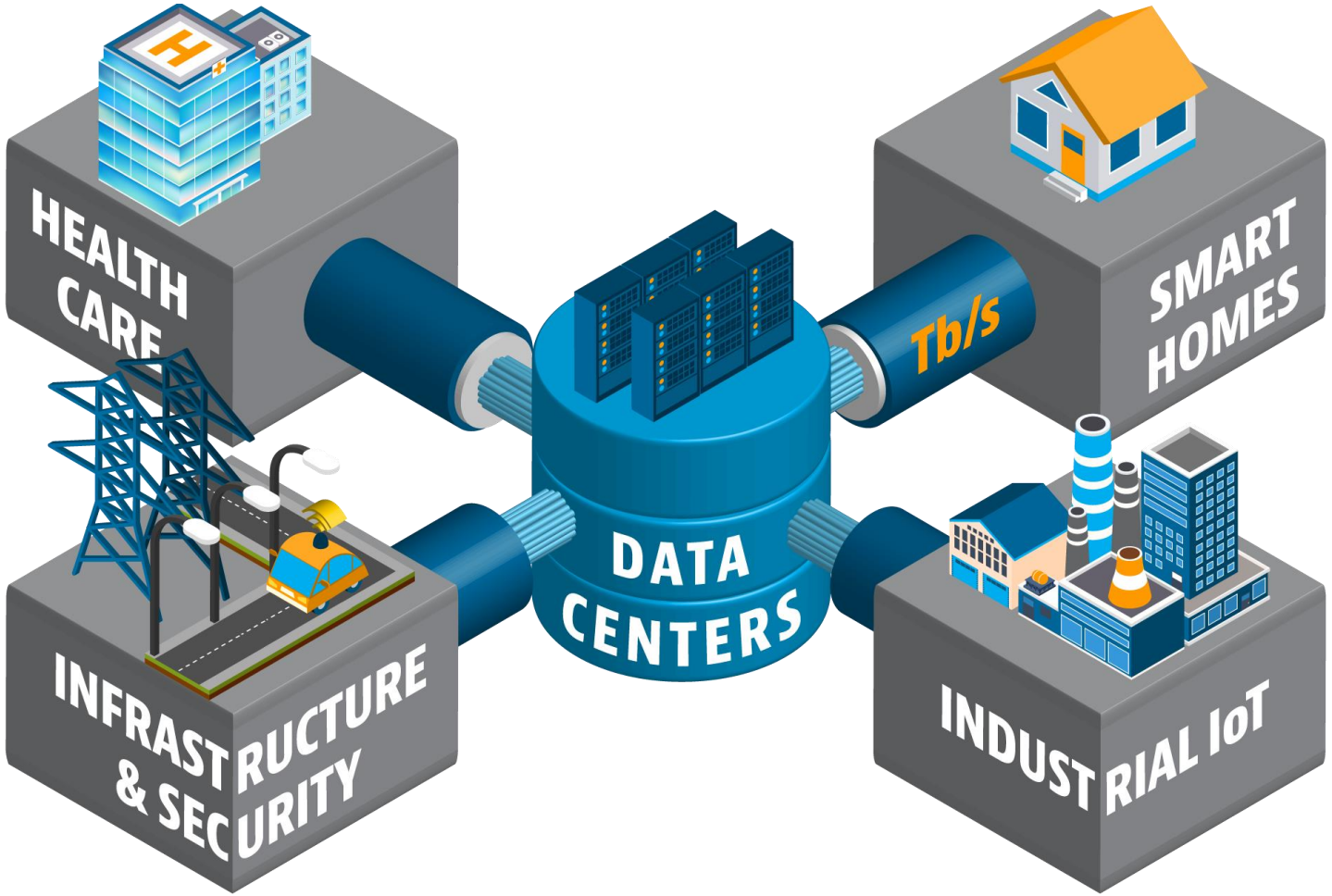
Ansys

This session

- Foundry-compatible Photonic Design Today (format: slides. 10 minutes)
  - Custom design: What is it and why is it challenging?
  - Process-enabled custom component design
  - Tower Semiconductor and Ansys foundry-compatible solution
- Design Case: Custom Ring Modulator for DWDM Transceiver (format: slides. 10 minutes)
  - Designing custom ring modulator using foundry process file
  - Calibrated compact model generation with CML Compiler
  - Circuit simulation with foundry components and custom components
- Walkthrough / Demo (format: Demo, slides. 60 minutes)
  - Step 1 – Working with Lumerical UI
  - Steps 2-5 – Photonic Component Simulation
  - Step 6 – Custom Compact models
  - Quick Mention (Step 7) – Photonic Circuit Simulation
- Q&A (10 minutes)

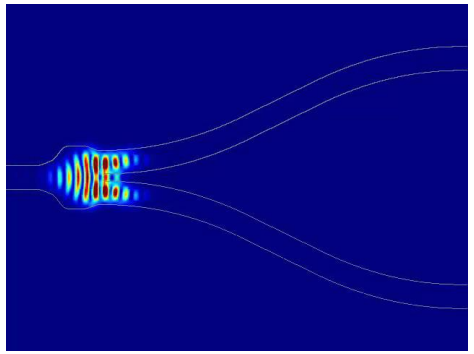
Custom Component Design for Photonic Integrated Circuit (PIC)

Photonics is Everywhere and Growing!

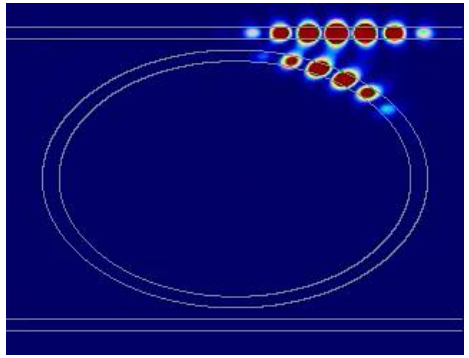


Building Blocks Beyond Waveguides

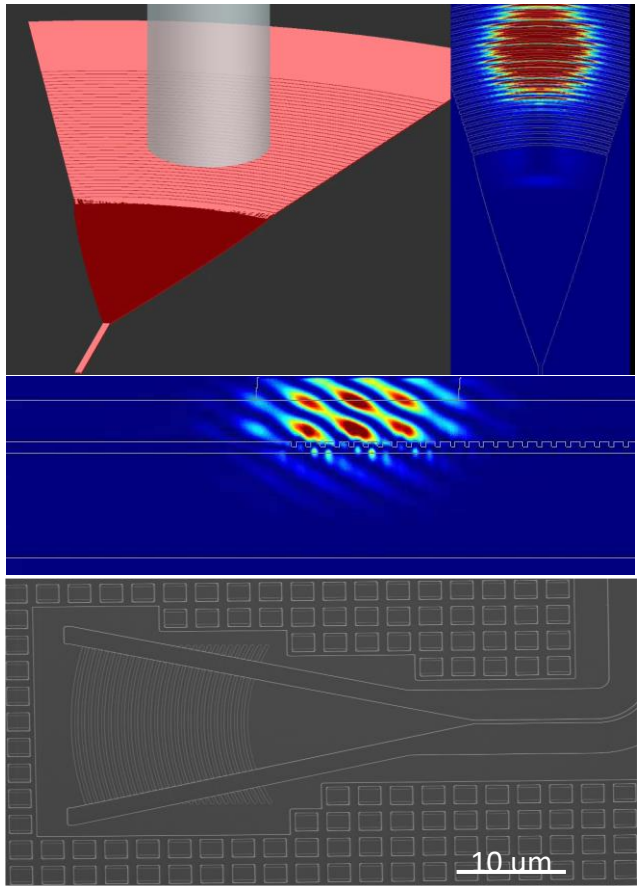
Waveguide coupling/splitting



Ring resonators

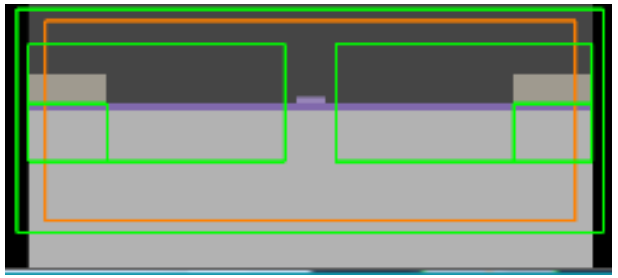


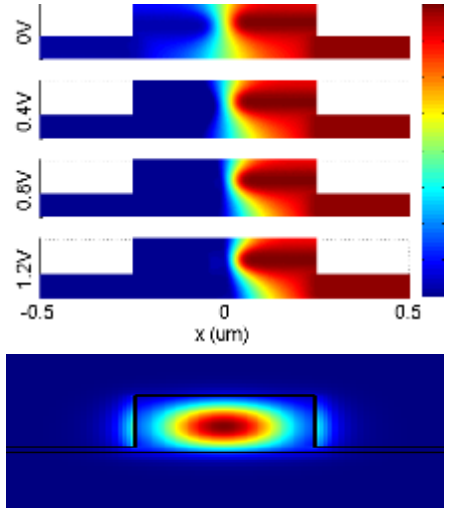
Fiber-waveguide coupling



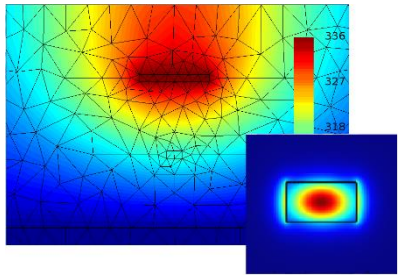
X. Wang: https://open.library.ubc.ca/collections/ubctheses/24/items/1.0165738

Electrical phase control

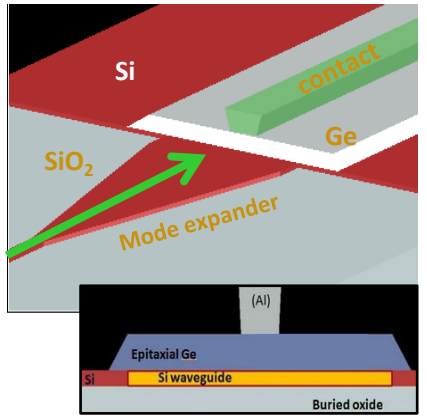




Thermal phase control



Photodetector



The two challenges of custom component design

1. **Creating the custom component according to the foundry’s process.**
2. **Creating the compact model for this the custom component.**

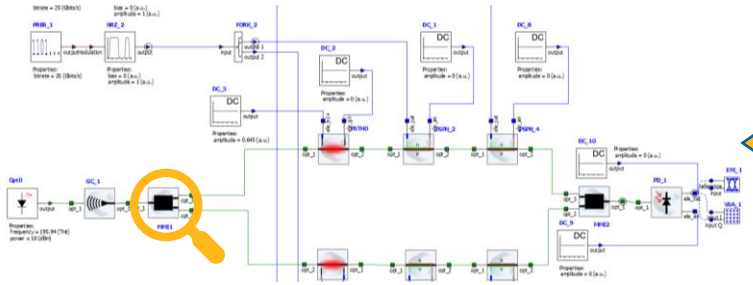
Why is Custom Design Challenging?

PDK
- Layouts
- CML
- Handbooks (technology, layout…)

Foundry

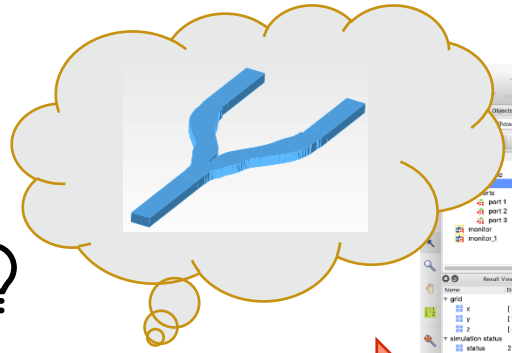
Circuit designer

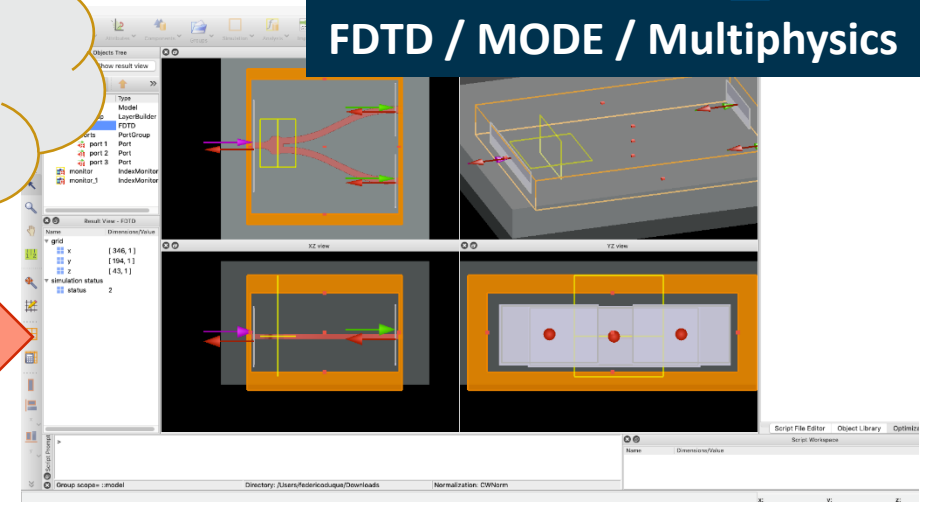
Circuit design with compact model library



Create compact models?

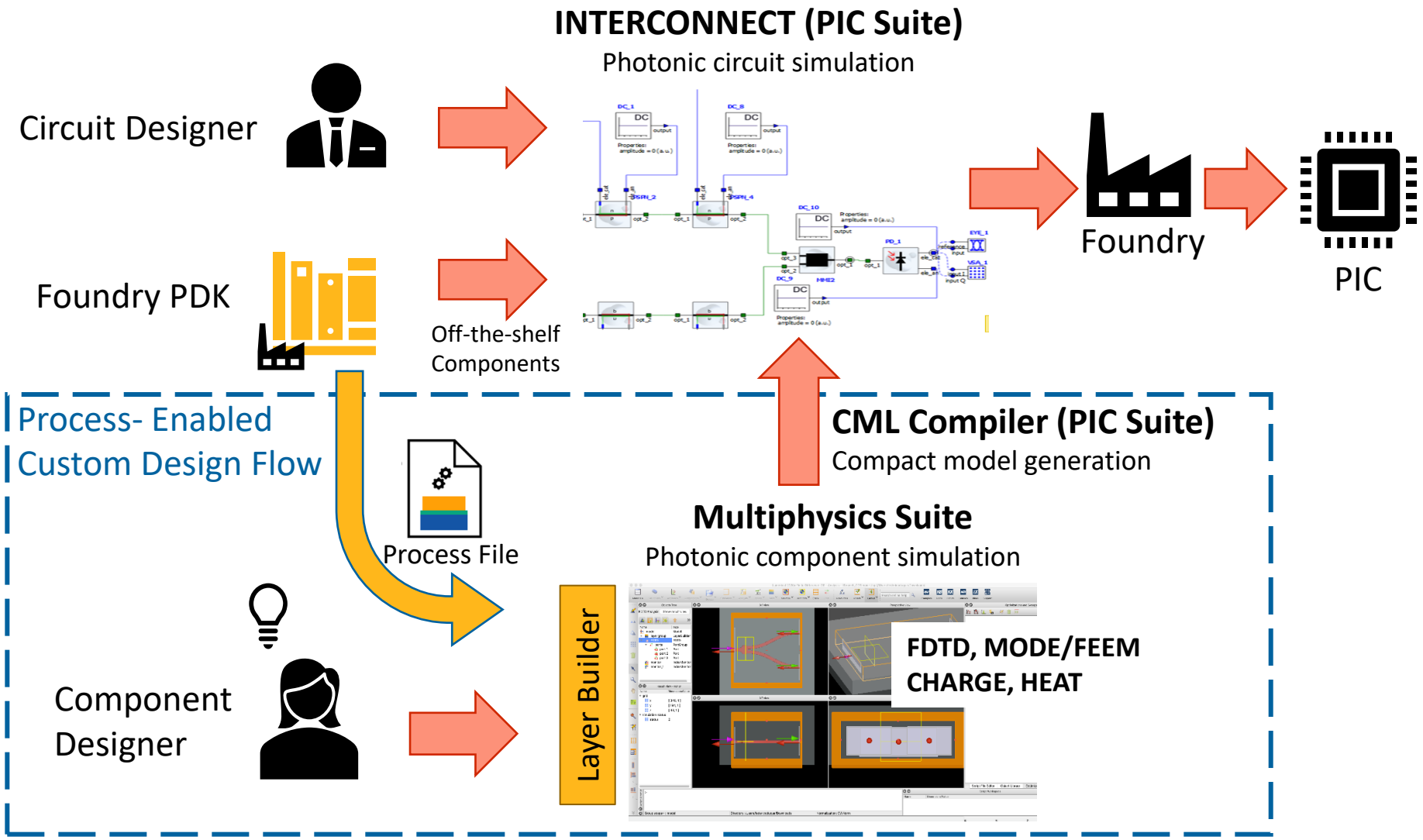
FDTD / MODE / Multiphysics





Component designer

Process-enabled Custom Component Design



https://www.ansys.com/blog/design-foundry-compatible-photonic-components

Foundry Process File Enables Active & Passive Component Design

Process Information

- Layer names and numbers
- Layer thicknesses
- Layer positions
- Material compositions

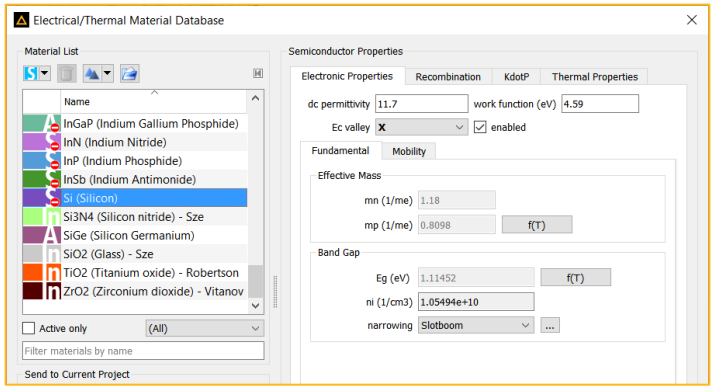
Layers

Geometry | Doping

enabled	name	layer number	start position (microns)	thickness (microns)
☑	Si_Substrate	None	-2	-10
☑	BOX	None	-2	2
☑	Si_CoreStripWG	1:0	0	0.22
☑	Si_SlabRibWG	1:1	0	0.09
☑	TOX	None	0	3.42

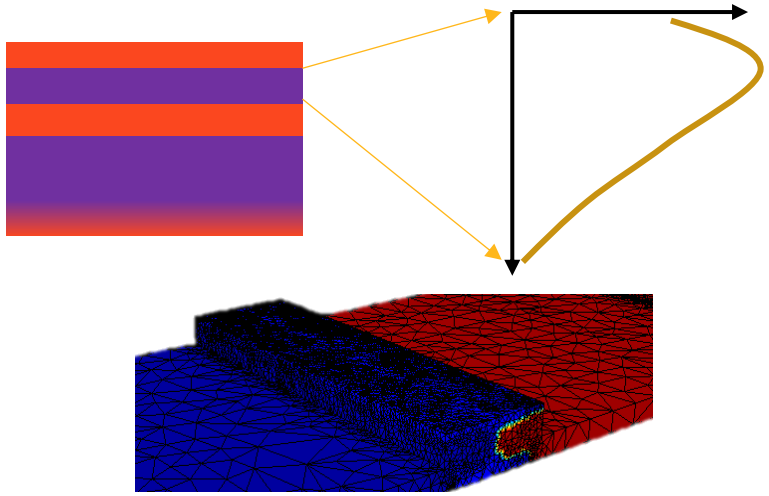
Material models

- Electrical material properties
- Thermal material properties
- Optical index perturbation models
  - Electrical + thermal stimulus

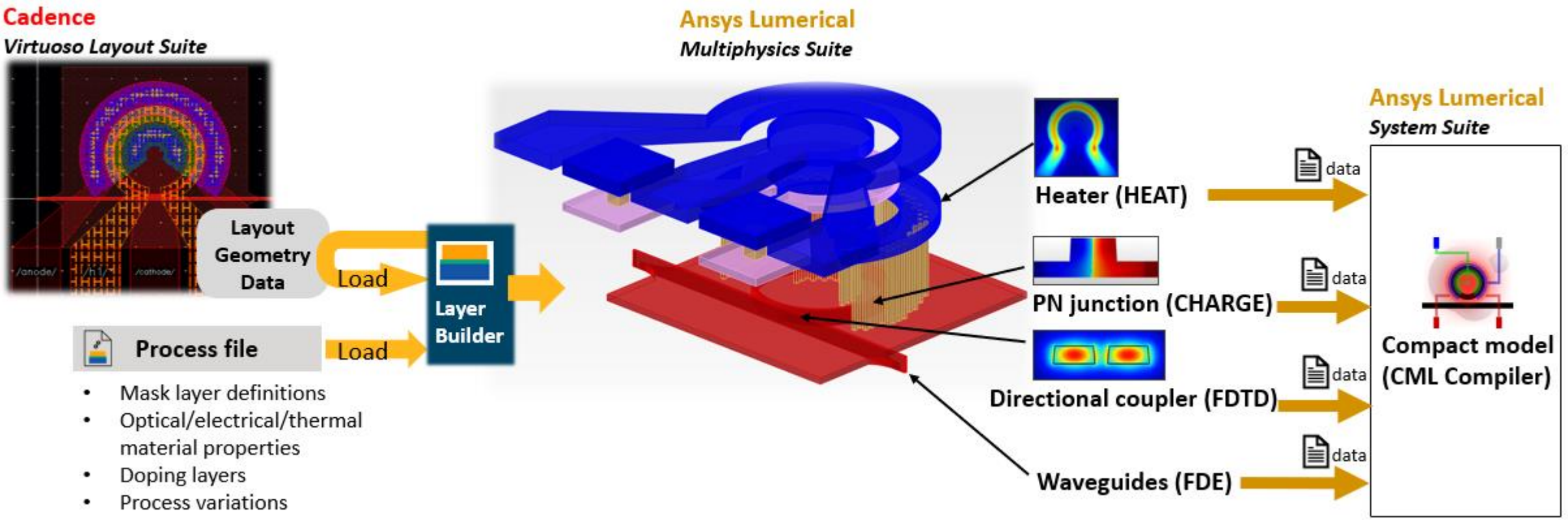


Doping profile

- Vertical 1D doping profile for each doping process
- Defined using normal or skewed normal distribution functions



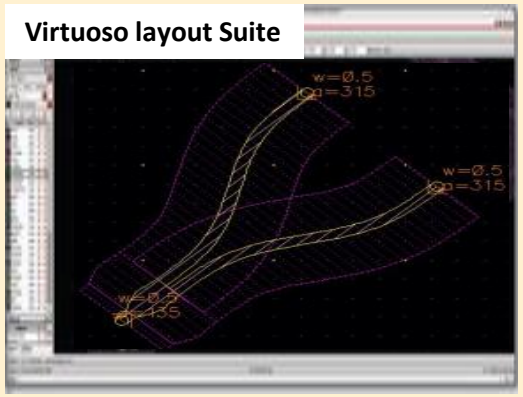
Design, Simulate, and Extract Component Model



Tower Semiconductor- Ansys Foundry Compatible Design Flow

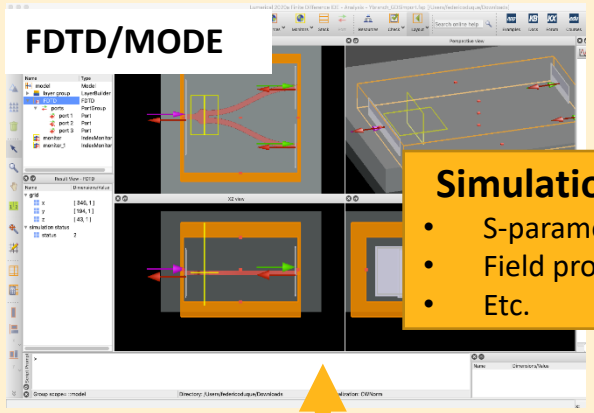
1. Device layout

Virtuoso layout Suite



2. Device simulation

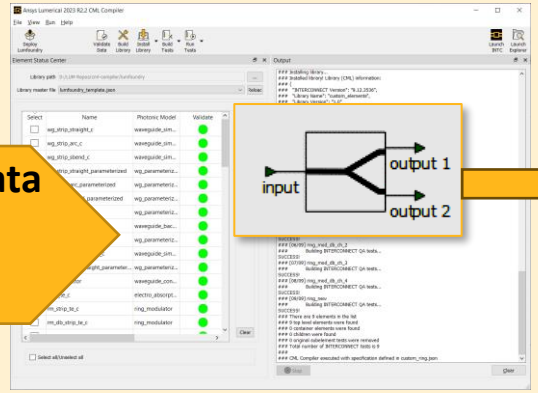
FDTD/MODE



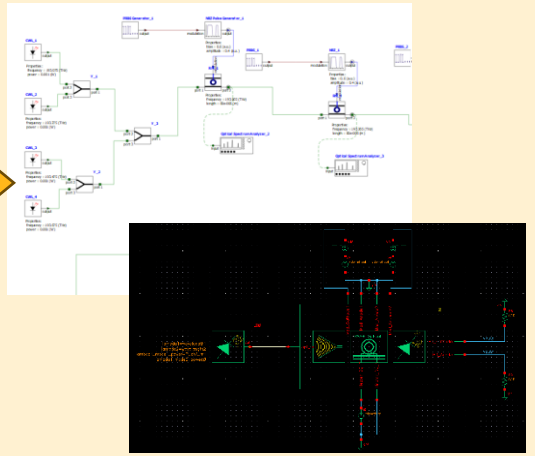
Simulation data

- S-parameters
- Field profiles
- Etc.

3. Compact Model Generation



4. Circuit Simulation



Direct bridge

LAYER BUILDER Build

Pcells and GDS files

Foundry process file with layer definition

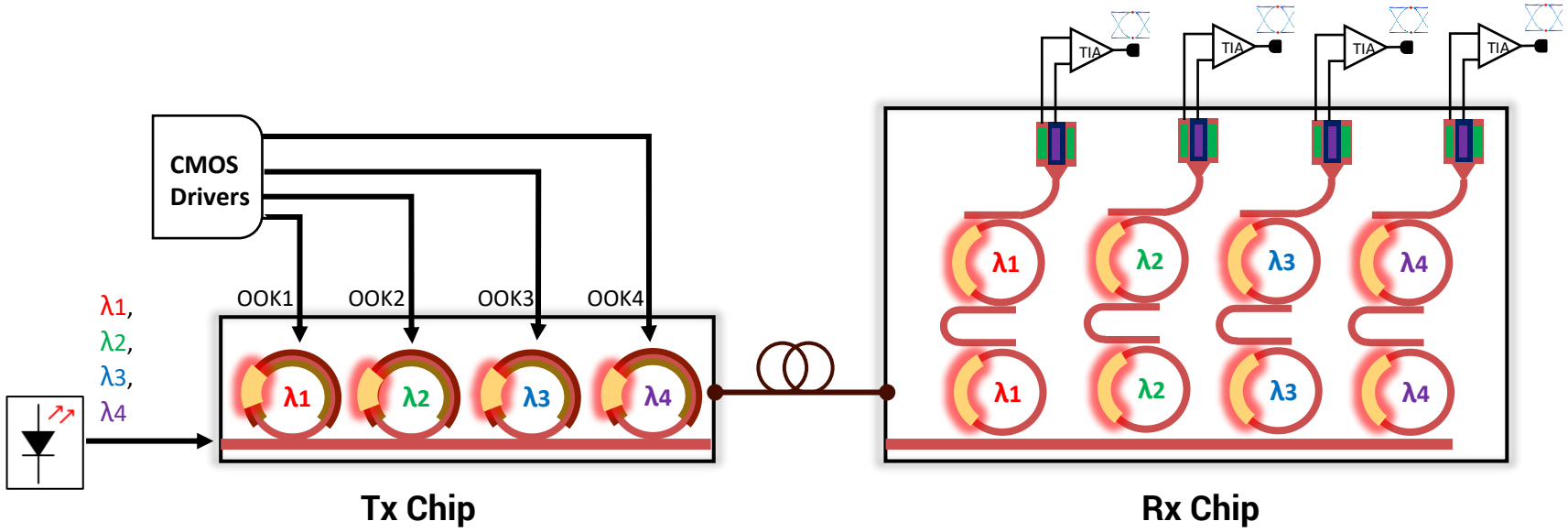
Compact model library (CML)

Tower Semiconductor PH18 PDK

Design of Ring Modulator and DWDM Circuit

Case Study

DWDM Circuit Simulation with Custom Ring Modulator

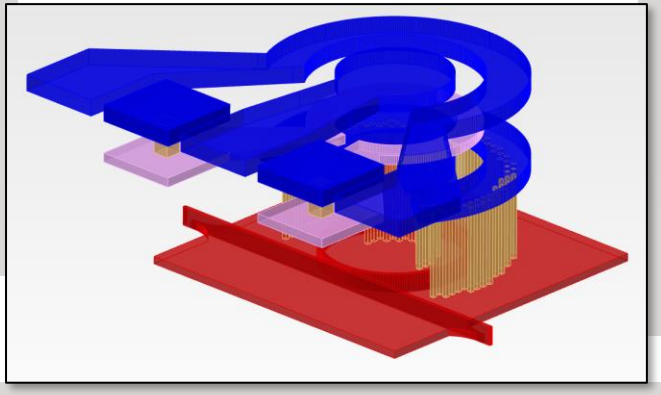


- DWDM (dense wavelength division multiplexing) is a popular method for designing photonic transceivers.
- 4-channel DWDM transceiver with CW lasers, transmitter circuit and receiver circuit.
- The key component is the ring modulator that encodes the RF signal onto the photonic carrier signal.
- **We will use our custom ring modulator along with other photonic components directly available in the Tower PDK to design and simulate the DWDM circuit.**

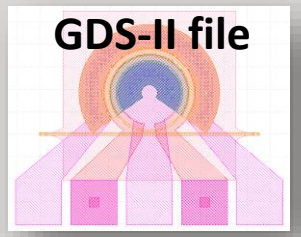
Ring Modulator Design Enabled by Foundry Process File

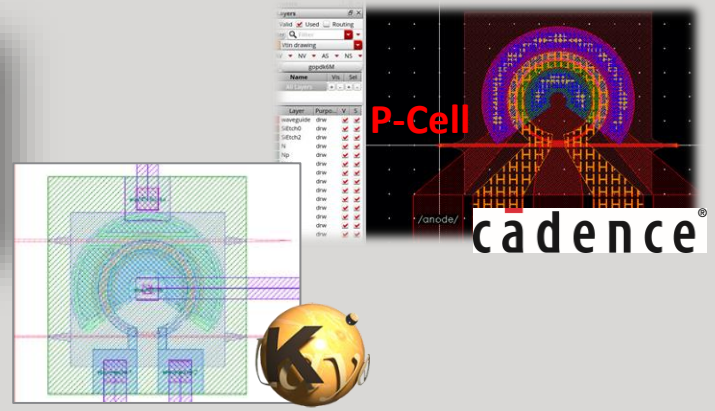
Process file

- Mask layer definitions
- Optical/electrical/thermal material properties
- Doping layers
- Process variations



Layout Geometry Data





Ansys Multiphysics Suite

FDTD: Directional Coupler

- Coupling coefficient

HEAT: Thermal tuner

- Temperature map
- Thermal Bandwidth
- Heater IV

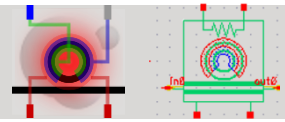
MODE/FEEM: Waveguides

- Effective index
- Group index

CHARGE: PN junction

- Charge distribution
- Slab Resistance
- Junction Capacitance

Ansys CML Compiler: Model data → Compact model



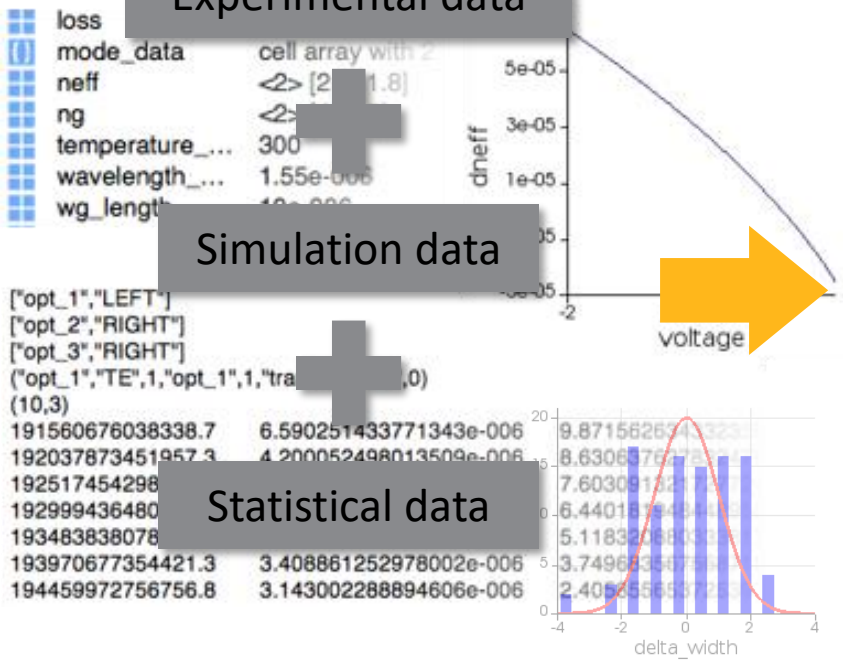
Compact Model Generation with CML Compiler

- ☑ **Accurate**
- ☑ **Calibrated**
- ☑ **Fabrication Variations**
- ☑ **Secure**
- ☑ **Frequently Maintained**

Experimental data

Simulation data

Statistical data

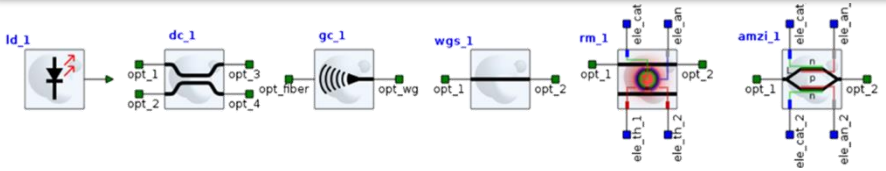


CML Compiler

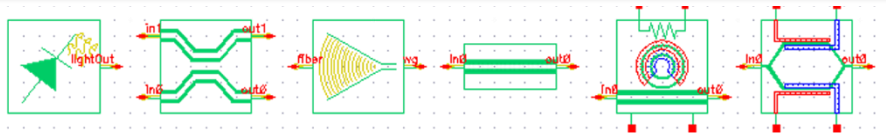
Photonic Models

Waveguides
Couplers
Photodetector
Modulators
etc.

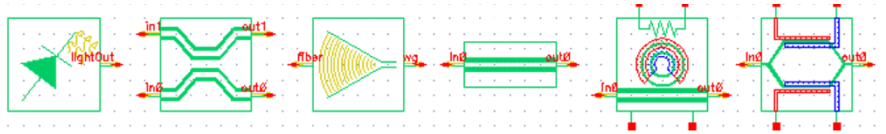
INTERCONNECT compact models



Virtuoso symbols



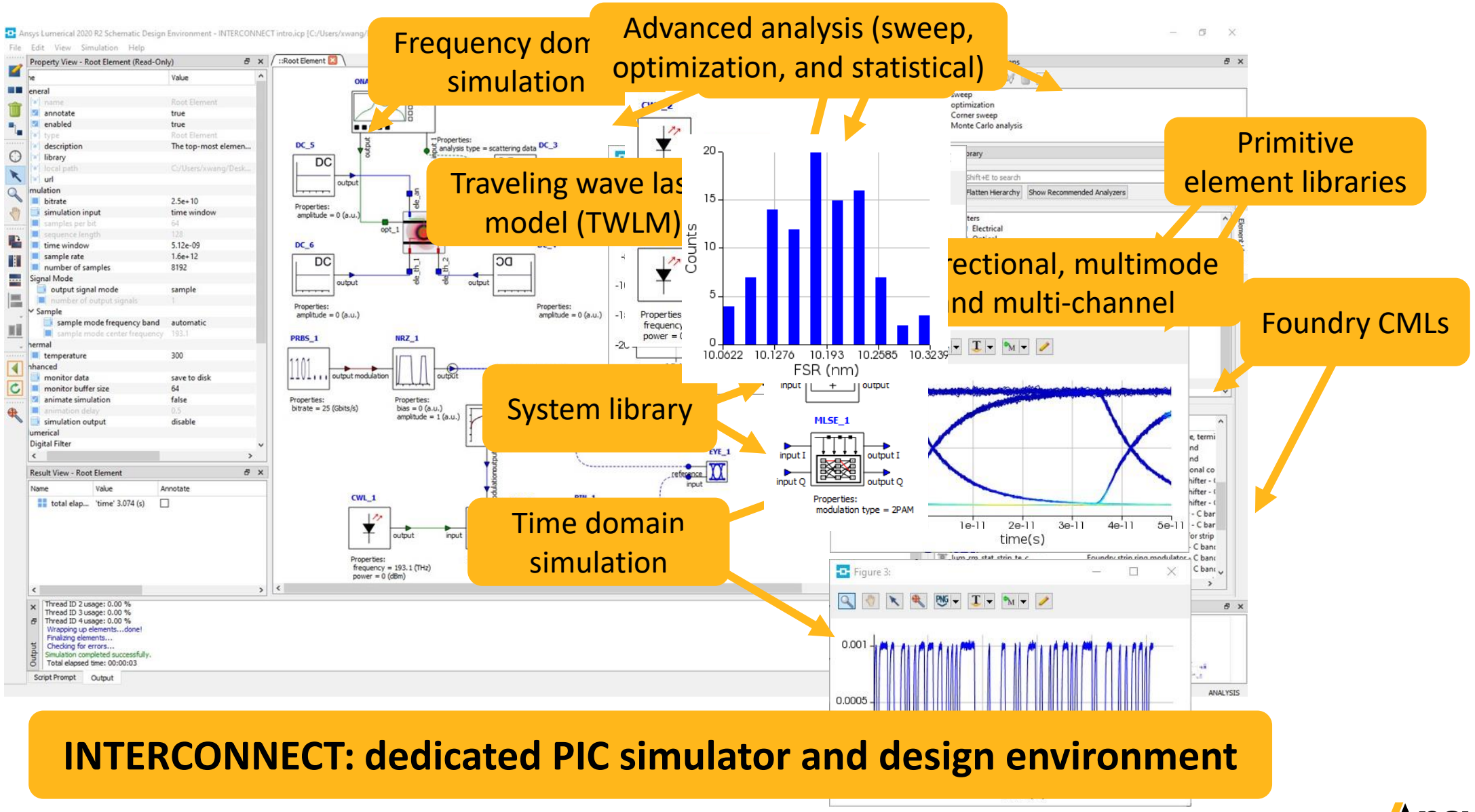
Photonic Verilog-A models (Spectre)



https://www.ansys.com/products/photonics/cml-compiler

https://optics.ansys.com/hc/en-us/articles/360037565953-CML-Compiler-product-reference-manual

DWDM Simulation with Lumerical INTERCONNECT



INTERCONNECT: dedicated PIC simulator and design environment

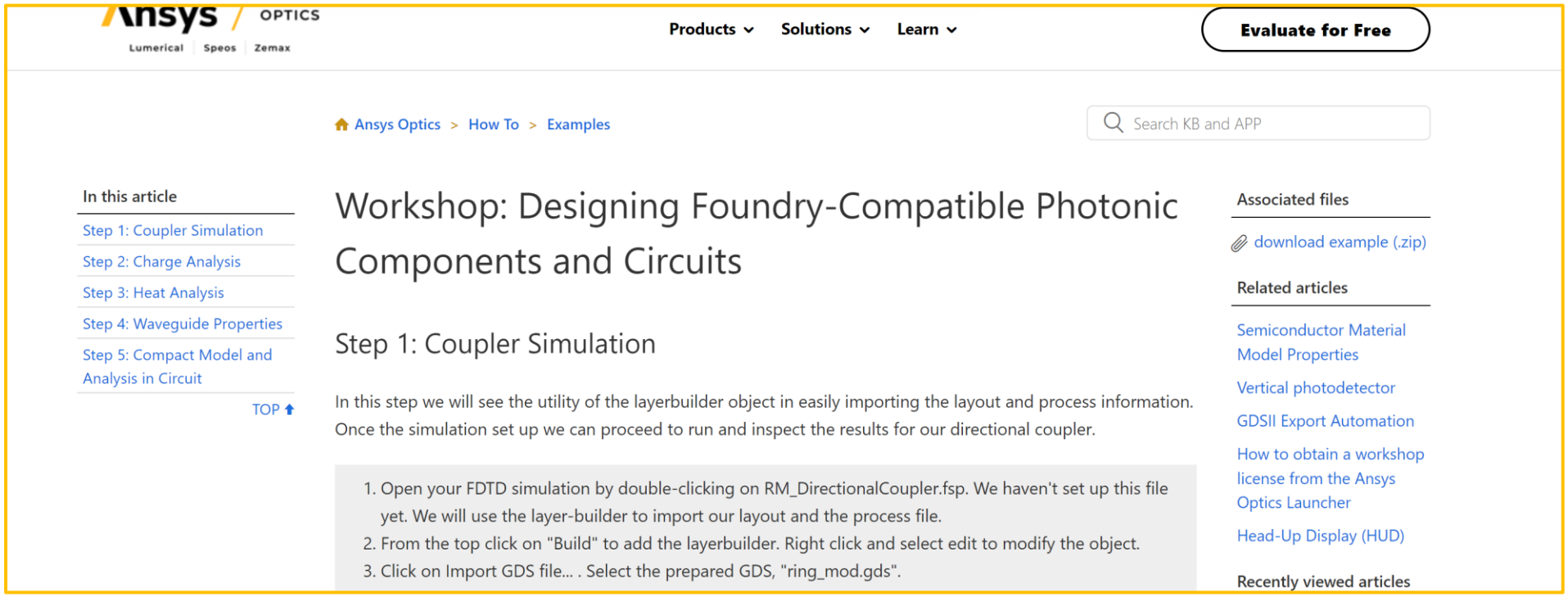
Walkthrough / Demo

Overview of the demo

- This workflow has been tested with Tower Semiconductor PH18M process file; however, the files here use a general process file.
- **6 steps demo to the design case mentioned earlier:**
  - **Step 1** – Becoming more familiar with Lumerical component level UI
  - **Step 2** – Directional coupler simulation with FDTD
  - **Step 3** – Modulator simulation with CHARGE
  - **Step 4** – Thermal modulation with HEAT
  - **Step 5** – Waveguide simulation with MODE
  - **Step 6** – Creating the compact model with CML Compiler
  - **Quick mention** – Circuit simulation with INTC

Testing this demo on your own

- The Workshop licenses, files, and steps to run will remain available until July 18th:
  - https://optics.ansys.com/hc/en-us/articles/31257798958611-Workshop-Designing-Foundry-Compatible-Photonic-Components-and-Circuits



Lumerical UI

Step 1

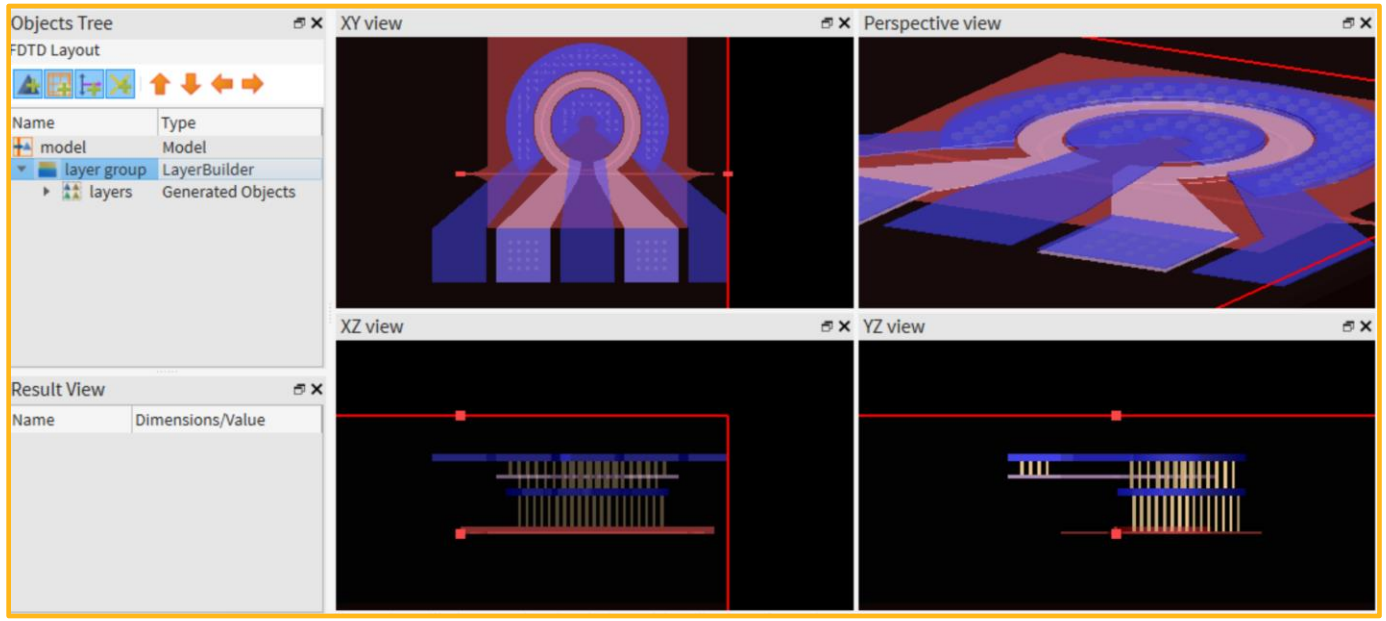
Tower Semiconductor
Where Analog and Value Meet

Coupler Simulation in FDTD

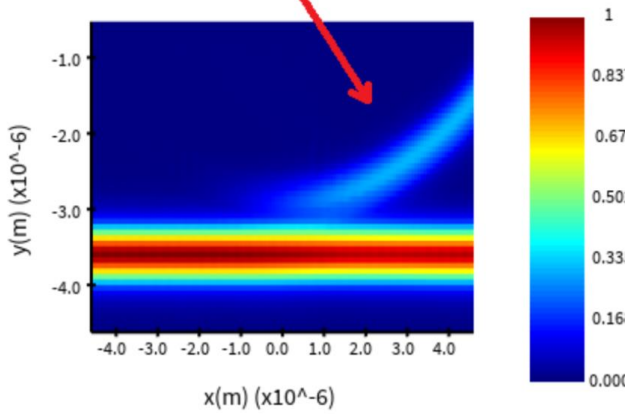
Step 2

Step 2: Directional Coupler Simulation with FDTD

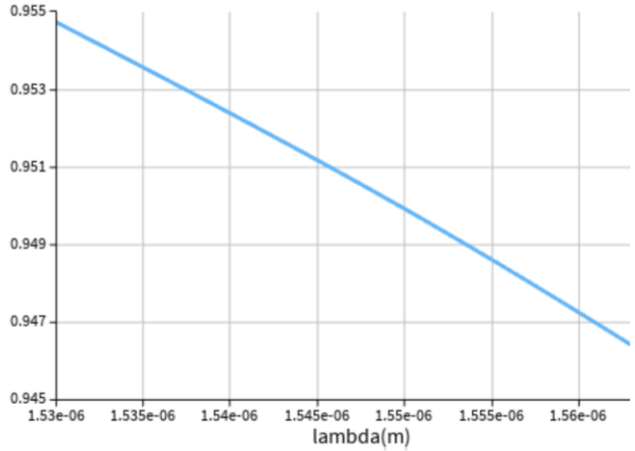
- 3D FDTD simulation using layer builder
  - Process file
  - GDS file for ring modulator design
- S-parameter sweep to extract coupling efficiency



E-field profile



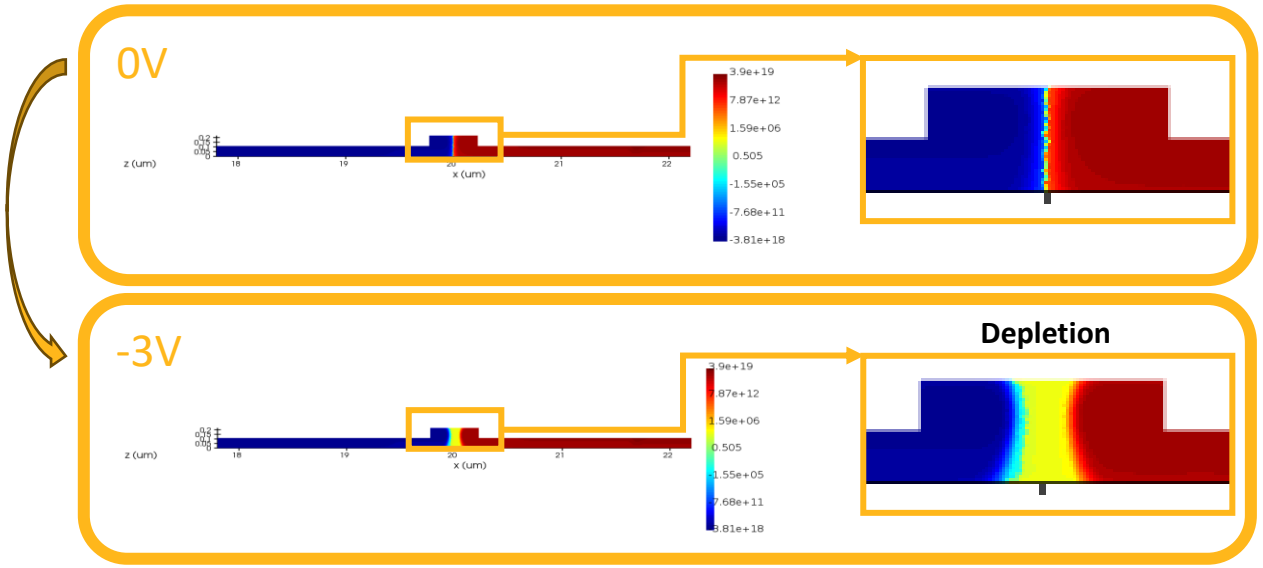
Through transmission

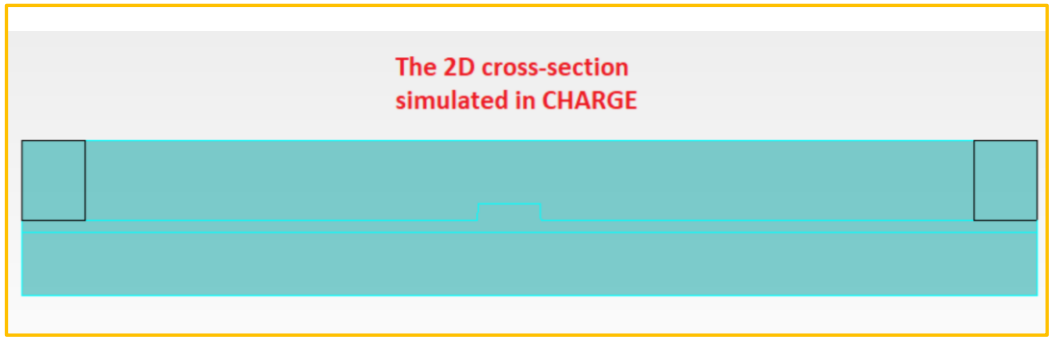


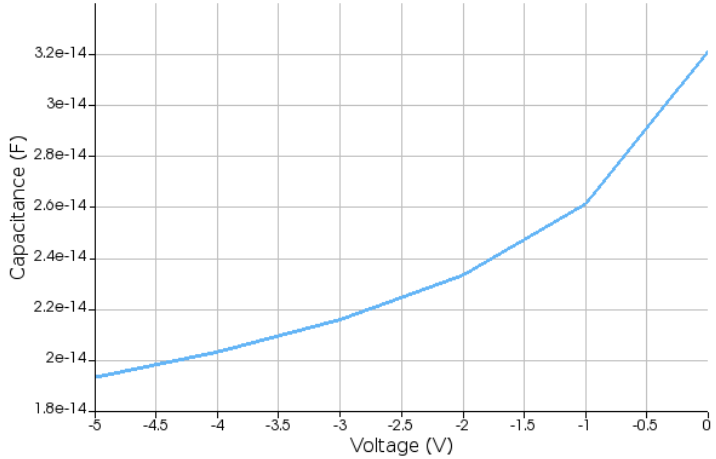
Modulator Simulation in CHARGE

Step 3

Step 3: PN Junction Simulation with CHARGE







- 2D CHARGE simulation using layer builder
  - Process file
  - GDS file for ring modulator design
- Bias voltage swept from 0 V to -3 V to extract charge density profile and electrical characteristic parameters

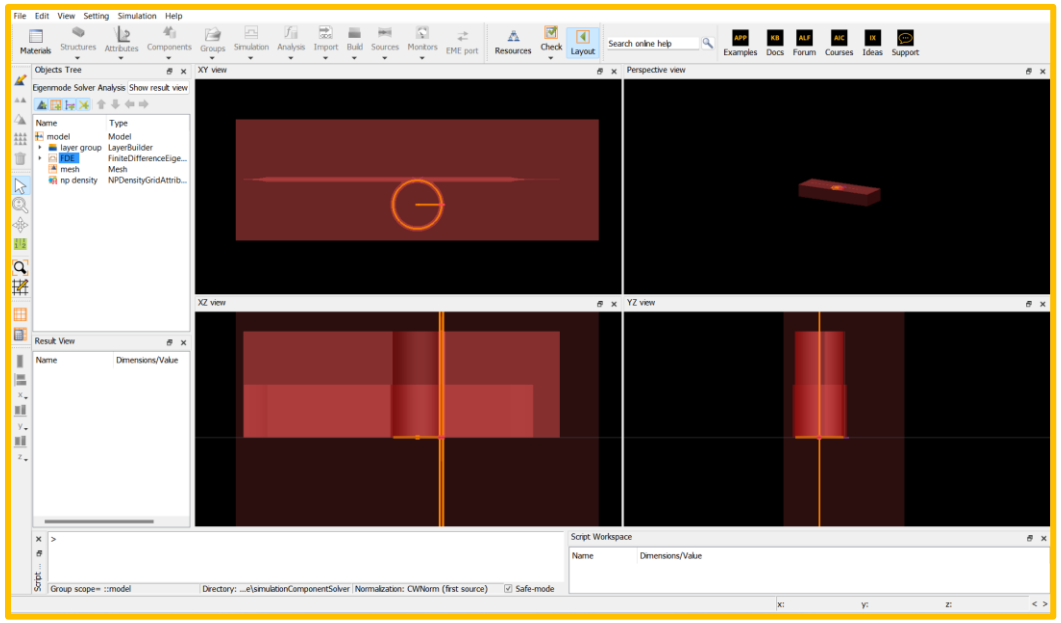
Thermal Simulation in HEAT

Step 4

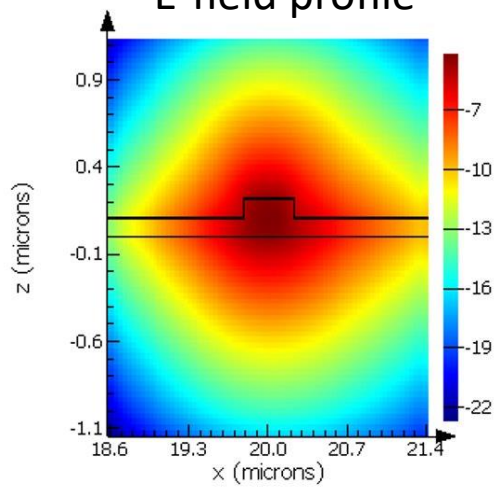
Waveguide Simulation in MODE

Step 5

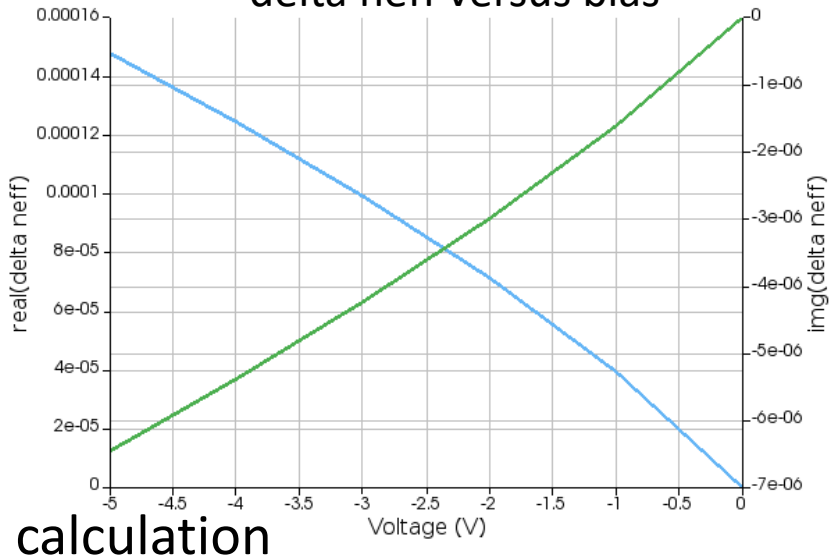
Step 5: Optical Waveguide Simulation with MODE



E-field profile



delta neff versus bias

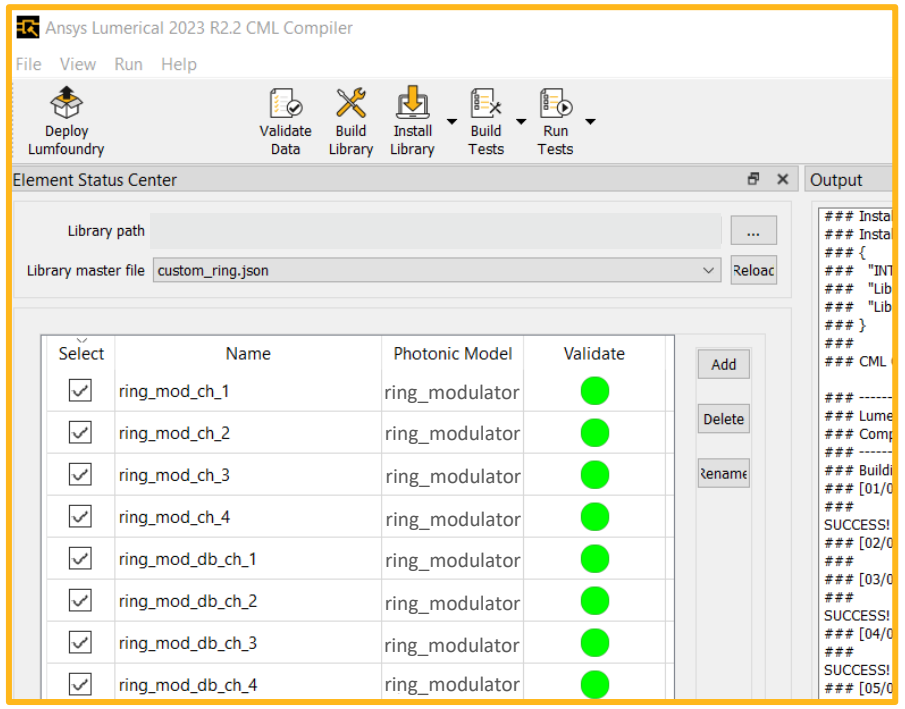


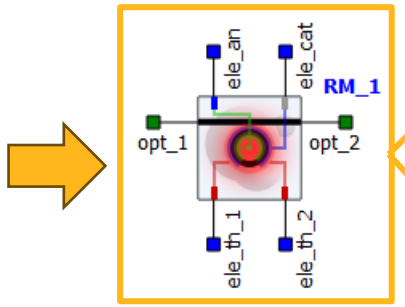
- 2D FDE simulation using layer builder
  - Process file
  - GDS file for ring modulator design
- Charge density profile imported from electrical simulation
- Bent waveguide analysis enabled for accurate mode profile calculation

Creating the Compact Model of your Device

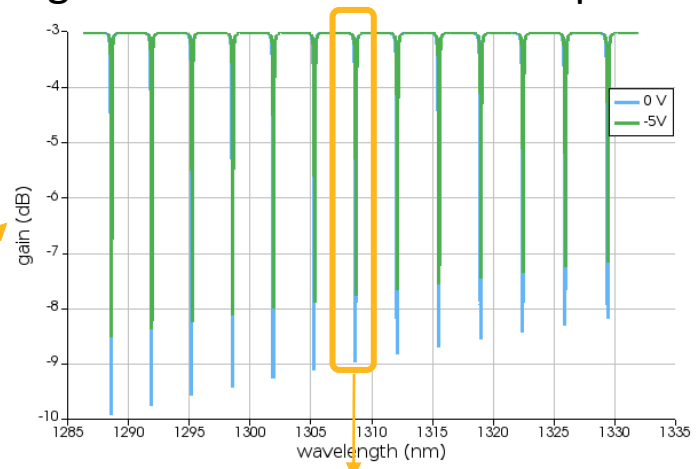
Step 6

Step 5: Ring Compact Model (CML Compiler → INTERCONNECT)

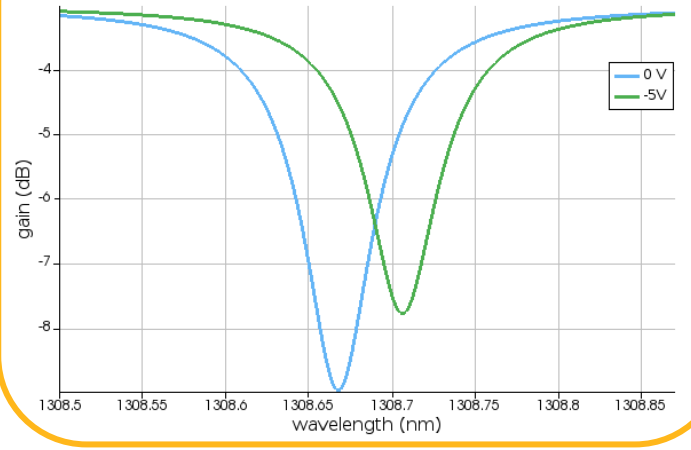




Ring modulator transmission spectra



Shift in resonance with applied bias



Step 5: Calibrated Ring Modulator Compact Model

- CML Compiler enables fine tuning of models based on measurement data.
- The ring_modulator model supports tuning for resonant wavelength, Q factor, FSR, IL, ER, thermal and electrical modulation efficiency.

```
"Q" :
{
  "max" : 40000,
  "min" : 20000,
  "tuning" : 0,
  "value" : 29885,
  "visible_to_user" : 0
},
"mod_eff" :
{
  "max" : 1.7e-11,
  "min" : 1.7e-11,
  "ref1" : 0,
  "ref2" : -5,
  "tuning" : 1,
  "value" : 1.7e-11,
  "visible_to_user" : 0
},
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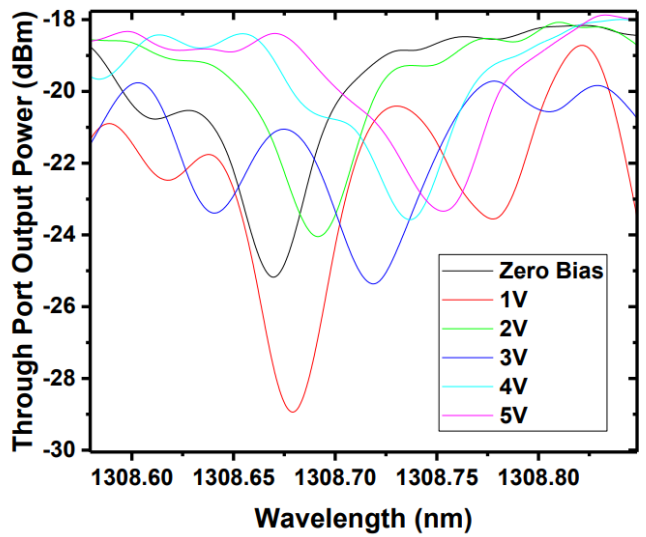
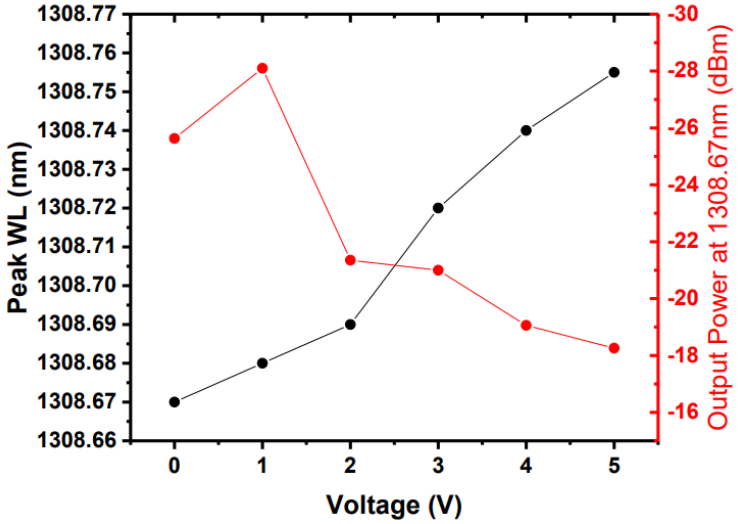


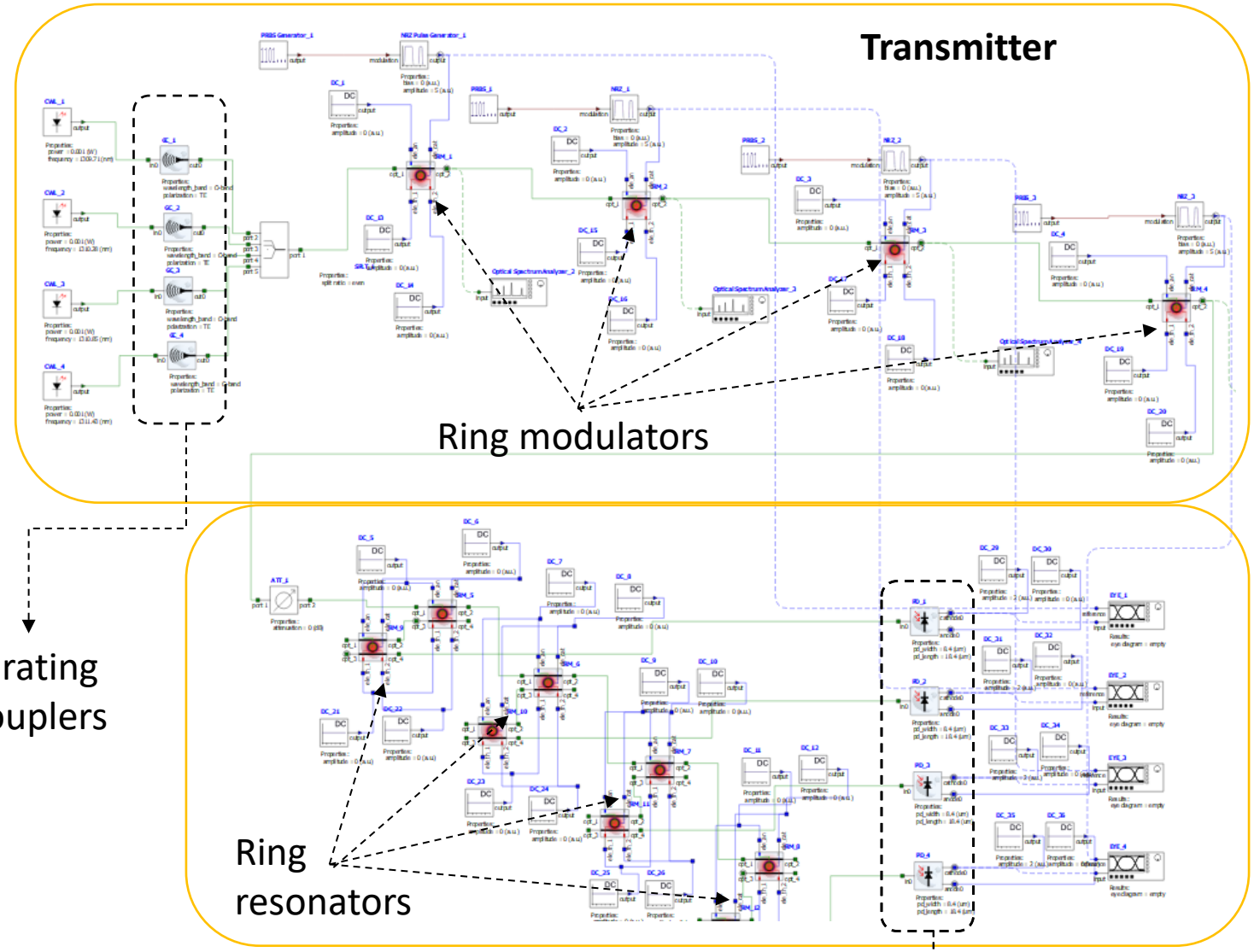


Enable ‘tuning’ to calibrate model with measurement data for various FOMs

Circuit Simulation with INTERCONNECT

Quick Mention
(Step 7)

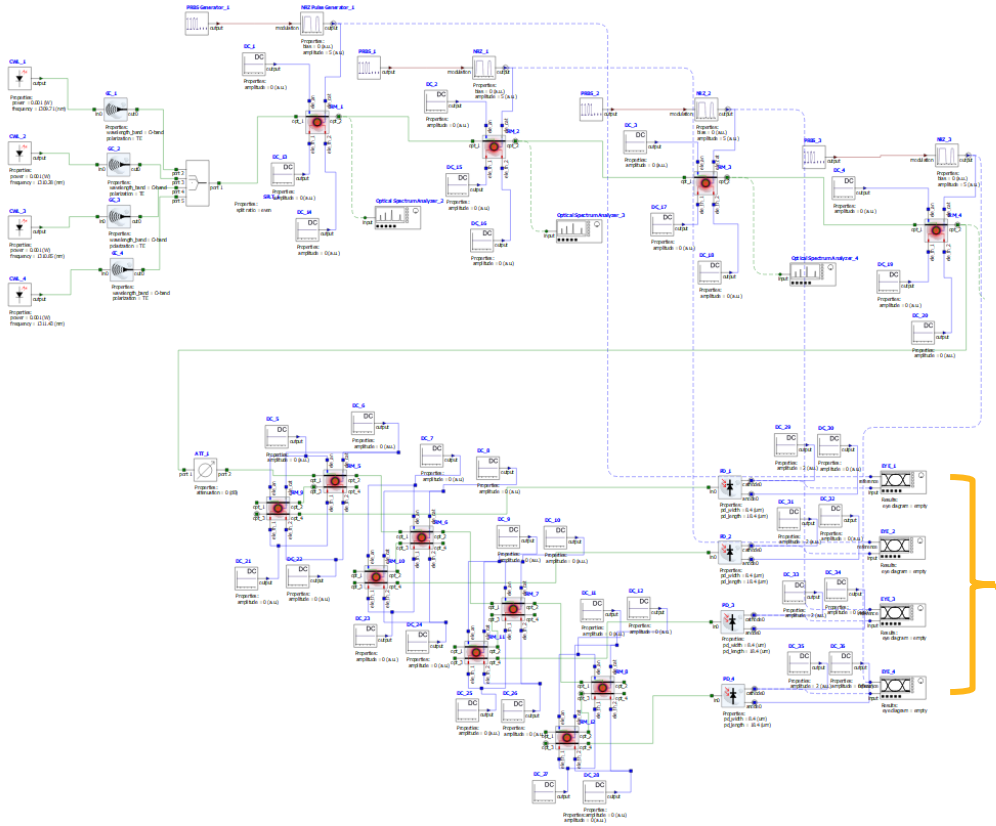
DWDM Circuit Simulation in INTERCONNECT



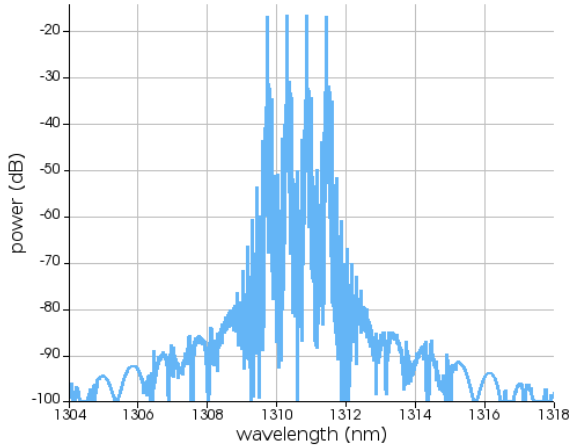
- 4-channel DWDM circuit with 100 GHz channel spacing.
- Grating coupler from the PH18 library to couple light from laser sources into the transmitting circuit.
- Custom ring modulator model from CML Compiler for the transmitter.
- Similar custom 4-port ring modulator/resonator for the receiver.
- Photodetector from the PH18 library to convert optical signal into electrical at the receiver end.

Circuit Simulation Results

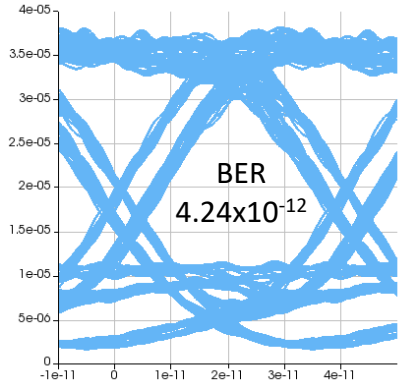
- Bitrate = 25 Gbps
- BER ≅ 10^{-12}

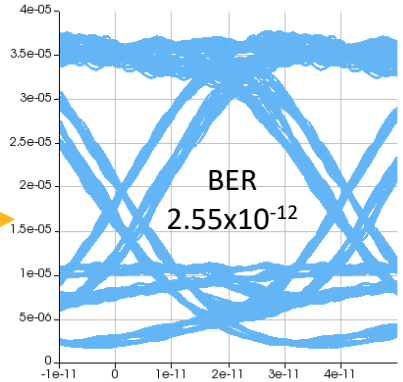


Transmitting spectrum

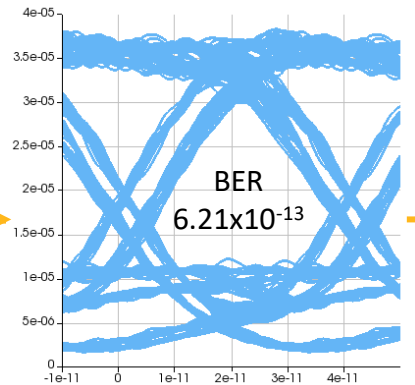


Channel 4

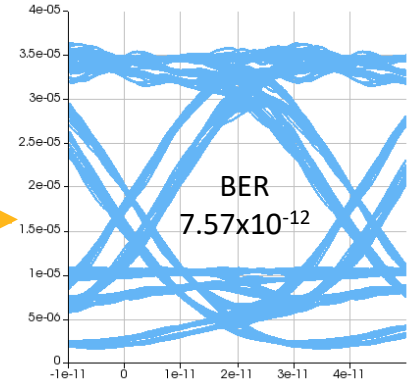




Channel 1



Channel 2



Channel 3

Summary

Summary

- Ansys and Tower Semiconductor have partnered to enable a complete electro-optic design flow for photonic designers.
- Ansys’s layer builder and Tower Semiconductor’s process file ensures accurate, foundry compatible design for both passive and active components.

Ansys

Q & A

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